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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/771,547
Filing Date: January 30, 2001
Appellant(s): SATO ET AL.

Manabu Kanesaka
Reg. No. 31,467
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 09/18/2006 appealing from the Office action mailed 05/18/2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The amendment after final rejection filed on 11/23/2005 has been entered.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,403,965 Ikeda et al.

2002/0163035 Yamazaki

Admitted prior art

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of Ikeda et al. (US Patent # 6,403,965).

[Claim 1]

Applicant's admitted prior art teaches a radiation detector comprising an active matrix board (Paragraphs 1-11, figures 2 and 3, element 10) including gate lines (4) and data lines (5) arranged in a two-dimensional lattice form, a plurality of high-speed switching elements (3) provided at respective lattice points and connected to the gate lines and the data lines, each having a source electrode, pixel electrodes connected to the source electrodes of the high-speed switching elements, and charge storage capacitances (2), each being disposed between the pixel electrode and a ground electrode (Paragraph 3) and a converting layer (1) formed on the pixel electrodes to generate a pair of electron-hole by absorbing one of light and radiation, said converting layer being formed of a vapor-deposited polycrystalline film of CdTe or CdZnTe (Paragraphs 3, 8 and 10, figures 2 and 3).

Applicant's admitted prior art does not explicitly teach that each high-speed switching elements are formed of poly-silicon thin film transistors.

However Ikeda teaches an X-ray image detector system wherein the TFTs may be formed of polysilicon (figures 1 and 2 show the TFT 701) in order to decrease the size of a TFT so that the effective area of each pixel can be increased (col. 12 lines 1-10).

Therefore taking the combined teachings of Applicant's admitted prior art and Ikeda, it would have been obvious to one skilled in the art at the time of the invention to have been motivated to have used poly-silicon as the material for TFTs in order to decrease the size of a TFT so that the effective area of each pixel can be increased as taught in Ikeda (col. 12 lines 1-10).

[Claim 4]

Applicant's admitted prior art teaches wherein said active matrix board (figure 2: 10) further includes a base plate (figure 2: 11) having high heat resistance and insulating property, an insulating film (figure 2: 2b) disposed on the base plate and sandwiched by the gate lines (figure 2: 4) and data lines (figure 2: 5), an insulating protecting layer (figure 2: 12) disposed on the insulating film above the switching element, and a common electrode (figure 2: 1b) disposed on the converting layer.

[Claim 7]

Applicant's admitted prior art teaches a radiation detector comprising an active matrix board (Paragraphs 1-11, figure 3, element 10) including gate lines (4) and data lines (5) arranged in a two-dimensional lattice form, a plurality of high-speed switching elements (3) provided at respective lattice points and connected to the gate lines and the data lines, each having a source electrode, pixel electrodes connected to the source electrodes of the high-speed switching elements, and charge storage capacitances (2), each being disposed between the pixel electrode

and a ground electrode (Paragraph 3) and a converting layer (1) formed on the pixel electrodes to generate a pair of electron-hole by absorbing one of light and radiation (Paragraph 8), said converting layer being formed of a vapor-deposited polycrystalline film of CdTe or CdZnTe having a film-forming temperature higher than 300C (Paragraphs 3, 8 and 10, figures 2 and 3).

Applicant's admitted prior art does not explicitly teach that each high-speed switching elements are formed of poly-silicon thin film transistors.

However Ikeda teaches an X-ray image detector system wherein the TFTs may be formed of polysilicon (figures 1 and 2 show the TFT 701) in order to decrease the size of a TFT so that the effective area of each pixel can be increased (col. 12 lines 1-10).

Therefore taking the combined teachings of Applicant's admitted prior art and Ikeda, it would have been obvious to one skilled in the art at the time of the invention to have been motivated to have used poly-silicon as the material for TFTs in order to decrease the size of a TFT so that the effective area of each pixel can be increased as taught in Ikeda (col. 12 lines 1-10).

3. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' admitted prior art in view of Ikeda et al. (US Patent # 6,403,965) in further view of Yamazaki (US PG-PUB # 2002/0163035).

[Claim 5]

Applicant's admitted prior art teaches a radiation detector-comprising gate driving circuit (figure 3: 6) to be connected to the gate lines (figure 3: 4), a signal driving circuit (figure 3: 7) to be connected to the data lines (figure 3: 5). Applicant's admitted prior art fails to teach a signal process circuit formed on the active matrix board for connecting the gate lines and data lines to

the gate driving circuit and the signal driving circuit. However Yamazaki teaches a signal processing circuits (figure 8: 702 and 703) formed on the active matrix board substrate (figure 8: 100) and connected to the pixel section 701 through gate wiring 704 and source wiring 158 (Paragraph 135). Therefore taking the combined teachings of Applicant's admitted prior art in view of Ikeda it would have been obvious to one skilled in the art at the time of the invention to have been motivated to have a signal process circuit formed on the active matrix board for connecting the gate lines and data lines to the gate driving circuit and the signal driving circuit as taught in Yamazaki in order to improve the operation performance and the reliability of a semiconductor device by properly using the TFT structures on the same substrate as taught in Yamazaki (Paragraph 19).

(10) Response to Argument

4. Appellant argues with regards to claim 1 (brief, page 7 and 8) that the rejection is in error because there is no suggestion or motivation in either Appellants' "admitted prior art" or Ikeda that would have led one to select the references and combine them in a way that would produce the invention defined by any of claims 1, 4 and 7. The Examiner respectfully disagrees.

Ikeda clearly teaches the motivation to use poly-silicon as the material for TFTs in order **to decrease the size of a TFT so that the effective area of each pixel can be increased. In addition, since the peripheral circuits can be prepared on the same glass substrate, it is possible to decrease the production costs including the costs for the peripheral circuits** (col. 12 lines 1-10).

5. Appellant argues with regards to claim 1 (Brief, page 9) that at the time the invention was made, an incompatibility between the heat resistance of TFT and the film forming temperature of

CdTe and CdZnTe was known to those knowledgeable in the art. Accordingly, it is not known to directly form a polycrystalline film of CdTe and CdZnTe on pixel electrodes, as recited in claims 1 and 7. The Examiner respectfully disagrees.

First, Paragraph 9 of the appellant's admitted prior art in the specification teaches that amorphous selenium (a-Se) as the converting layer 1 is directly formed on the active matrix board 10. Appellant's admitted prior art goes on to explain in paragraph 10 that if a polycrystalline film of CdTe and CdZnTe as a converting layer 1 instead of amorphous selenium (a-Se) is formed directly on pixel electrodes, a film forming temperature higher than 300 degrees C. is required but the active matrix board which is made of TFT (thin-film transistor) amorphous silicon (a-Si:H) pose a problem because of the limited heat resistant temperature of 250 degrees Celsius.

Therefore reading paragraphs 9 and 10 following materials were used as prior art

a) Converting layer 1 → amorphous selenium (a-Se) or polycrystalline film of CdTe and CdZnTe.

b) Active matrix board → TFT (thin-film transistor) amorphous silicon (a-Si:H).

Problems that are associated with using these materials.

a) To form a layer of polycrystalline film of CdTe and CdZnTe as a converting layer instead of amorphous selenium (a-Se), a film forming temperature higher than 300 degrees C. is required and the active matrix board which is made of amorphous silicon (a-Si:H) pose a problem because of the limited heat resistant temperature of 250 degrees Celsius.

To combat this problem, the heart of the appellant's invention is to use the switching elements 3 made of poly-crystalline silicon having a film-forming temperature of more than 300 degrees C as explained in Paragraph 29 of the appellant's specification.

As claimed in claim 1, Appellant's invention lies in the claimed limitation "each switching element being formed of a polycrystalline silicon thin film transistor" as recited in lines 4-6 of claim 1. The rest of the claim has been taught in Appellant's admitted prior art.

Ikeda clearly teaches an X-ray image detector system wherein the TFTs as switching elements may be formed of polysilicon (figures 1 and 2 show the TFT 701) in order to decrease the size of a TFT so that the effective area of each pixel can be increased. In addition, since the peripheral circuits can be prepared on the same glass substrate, it is possible to decrease the production costs including the costs for the peripheral circuits (col. 12 lines 1-10). Ikeda also explains each of the pixels 801 comprises a switching element 701 using a thin film transistor (col. 5 lines 61-65, figures 1 and 2).

6. Appellant argues with regards to claim 1 (Brief, Pages 9 and 10) that Ikeda teaches in column 12 lines 1-10 lines instead of amorphous silicon, polysilicon can be used, but the purpose of using polysilicon is to reduce the size of the TFT. In the present invention, since the heat resistance of the active matrix board using polysilicon is high to withstand the formation of CdTe and CdZnTe, polysilicon is used. In Ikeda, polysilicon is used only for reducing the size of TFT. Further, even if polysilicon is used in Ikeda, the Se films for the X-ray-to-charge converting part are still deposited on the TFT. Therefore, the detector system in Ikeda is different from the present invention, as a whole. The Examiner respectfully disagrees.

MPEP 2144 states that the reason or motivation to modify the reference may often suggest what the inventor has done, but for a different purpose or to solve a different problem. It is not necessary that the prior art suggest the combination to achieve the same advantage or result discovered by applicant. *In re Linter,* 458 F.2d 1013, 173 USPQ 560 (CCPA 1972). Although *Ex parte Levengood,* 28 USPQ 2D 1300, 1302 (BPAI 1993) states that obviousness cannot be established by combining references "without also providing evidence of the motivating force which would impel one skilled in the art to do what the patent applicant has done", reading the quotation in context it is clear that while there must be motivation to make the claimed invention, there is no requirement that the prior art provide the same reason as the applicant to make the claimed invention. Therefore Ikeda's motivation for using an X-ray image detector system wherein the TFTs as switching elements may be formed of polysilicon is **to decrease the size of a TFT so that the effective area of each pixel can be increased. In addition, since the peripheral circuits can be prepared on the same glass substrate, it is possible to decrease the production costs including the costs for the peripheral circuits** (col. 12 lines 1-10) is found to be sufficient.

7. Similar arguments apply to claim 7.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Yogesh K Aggarwal/

Examiner, Art Unit 2622

May 13, 2009

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